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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,321	01/18/2002	Santosh C. Lolayekar	E003 - 1000US1	7045

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ART UNIT	PAPER NUMBER
2152	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/051,321	LOLAYEKAR ET AL.
	Examiner	Art Unit	
	Chad Zhong	2152	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>17 October 2005</u>.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-44* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-44* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

FINAL ACTION

1.   In response to amendment filed 10/17/2005, claims 1-44 are pending for examination. Examiner

notes that claims 1, 9, 20, 24, 35, and 42 are currently amended. Applicant's arguments are not

persuasive, and the previous rejections are maintained. In addition, newly rejections cited are stated

below.

2.   It is noted that although the present application does contain line numbers in specification and

claims, the line numbers in the claims do not correspond to the preferred format. The preferred format is

to number each line of every claim, with each claim beginning with line 1. For ease of reference by both

the Examiner and Applicant <u>all</u> future correspondence should include the recommended line numbering.

3.   Applicant is required to update the status (pending, allowed, etc.) of all parent priority

applications in the first line of the specification. The status of all citations of US filed

applications in the specification should also be updated where appropriate.

Claim Analysis

4.   As per claim 1, examiner will interpret the claim as follows. A node within a network having

plurality of line cards with ports and storage protocol processing units, each units will process storage

commands received at the ports. Applicant does not explicitly teach in the specification what is meant by

"storage protocol", in light of the specification and what is known in the art, storage protocol will be

interpreted as protocol used for accessing storage devices, SCSI and Fiber Channel are known in the art as

storage protocols used for storage access.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United
States before the invention thereof by the applicant for patent, or on an international application by another who has
fulfilled the requirements of paragraphs (1), (2), and (4) of section 371 (c) of this title before the invention thereof by
the applicant for patent.

6.   Claims 1, 4, 5, 8, 15, 18, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by

Blumenau et al. (hereinafter Blumenau), US 6,438,595.

7.   As per claim 1 Blumenau teaches a switch for use in a network, comprising:

a plurality of linecards (Col. 5, lines 12-20, where there are at leas two types of line cards, one

being the port adapter and the other being the storage adapter), each including:

a plurality of ports (Fig. 1, item 35 and 36); and

a plurality of storage protocol processing units (Col. 5, lines 12-27, where the storage adapters

handles the *communications protocol of the storage devices* - emphasis added, each of the storage

adapters has processors for handling the communications protocol of the storage devices, that is,

Blumenau discloses *communications protocol of the storage devices* are FWD SCSI or Fibre Channel

fiber-optic loops both are well known storage protocols), wherein each storage protocol processing unit is

associated with at least one port and performs storage command processing for commands received at

said at least one port (Col. 4, lines 37-54, Col. 5, lines 12-30, where storage adapters and port adapters are

closely associated with each other, in order to effectively read and write information to and from cache

and storage volumes), thereby distributing processing resources amongst linecard ports.

8.   As per claim 4, Blumenau teaches each linecard is designed to handle packets formatted in

accordance with any respective one of a plurality of protocols (Col. 5, lines 23-31).

9.   As per claim 5, Blumenau teaches:

a first set of linecards in the plurality is designed to send and receive packets in accordance with

an iSCSI protocol (Col. 5, lines 20-27); and

a second set of linecards in the plurality is designed to send and receive packets in accordance

with a Fibre Channel protocol (Col. 5, lines 20-27).

10.   As per claim 8, Blumenau teaches the switch is capable of receiving a packets at wire speed (Fig.

1-3, Col. 5, lines 25-30).

11.   As per claim 15, the claim is rejected for the same reasons as rejection to claim 1 above,

additionally, Blumenau teaches a switch for use in a network, comprising:

processing units associated with a memory (Col. 5, lines 15-22, where the storage adapter's

processing units are associated with storage drives, storage drives are a form of memory);

a CPU in communication with the processing units (Col. 5, lines 15-22, where each adapter cards

posses hardware/software logic to handle the read/write requests from the network, the CPU as claimed is

equivalent to the 'one or more' processors for handling such tasks); and

a fabric in communication with each linecard (Col. 6, lines 50-60; Fig 2, item 35, 36, and 40,

where the adapter/linecards are connected to the port switch, which in turn provides fabric in

communication with each linecard), thereby allowing packets to pass from an ingress linecard to an egress

linecard.

12.   As per claim 18, Blumenau teaches the associated memory is associated with each processing

unit (Col. 4, lines 37-54).

13.   As per claim 21, Blumenau teaches a switch for use in a system for storing and accessing data the

switch comprising:

a plurality of linecards, each linecard including:

at least one port, and

means associated with each port for performing wire speed processing of packets (Col. 5, lines 13-31, Fig 1-3, where the wire speed here is in accordance with the line speed of the network, the processing speed is restricted by links between disks and storage adapters, i.e. FWD SCSI or Fiber Channel fiber-optic loops each have different speeds of access).

13.   Claim 20, 35, 40-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen et al. (hereinafter Nguyen), US 2002-0004883.

14.   As per claim 20, Nguyen teaches a switch for use in a system for storing and accessing data, the switch comprising:

a plurality of linecards, each linecard including:

at least one port ([0027], [0040], ports would be opened for network access) and a plurality of processing units ([0027], processing units are DP 1 through DP 9), wherein each processing unit is associated with at least one port ([0027], each DPs need a port to access remote TDs), and each processing unit includes a classifier, a virtualizer, and a translator ([0027], wherein the classifier, virtualizer and translator are achieved using data processors DP 1 through DP 9, though in one embodiment they are separate entities, however, in another embodiment, DP1-DP4 have functionalities of CB1-CB4, meaning they are integrated together into one unit and functionalities of CB1-CB4 are included within each of DP1-DP4, thus, Nguyen teaches processing units DP1-DP9 includes a classifier, a virtualizer, and a translator);

a first CPU in communication with each processing unit ([0027], where ACSC can be seen as the first CPU and processing units are combination of DP1-DP4 and CB1-CB4, the ACSC's CPU is in communications with each of the DP1 through DP4; alternately, each of combination of DP1-DP4 and

CP1-CB4 can be seen as the CPU and CB5-CB9 can be considered as processing unit. Specifically, the

translation from physical to virtual device can occur in connection blocks CB5-CB9 and in this case CB1-

CB4 serve as a pass through function, where CB5 would serve the same function as CB-1 and CB-1 will

act as a pass through device for the DP1 processor CPU); and

      a fabric in communication with each linecard ([0032]).

15.   As per claim 35, Nguyen teaches a storage network comprising:

      a switch ([0027], switch is a combination of CP1 and CB1-CB4);

      a server in communication with the switch, the server operating in accordance with a first

protocol ([0027], server is the combination of NSM/ACSC controller and CB0);

      a storage device in communication with the switch, the storage device operating in accordance

with a second protocol ([0027], storage devices are TD1-TD4);

      the switch having an input for receiving data for a virtual target formatted in accordance with the

first protocol ([0027], where the DP1 sends data to remote target TDs through CB1-CB4); and

      the switch having an output for sending data for a virtual target formatted in accordance with the

first protocol at wire speed ([0027], in one embodiment, CB1 will act as a forwarding unit to forward the

command to CB5, therefore, no buffering is done at the switch side, there are no store and forward at the

switch).

16.   As per claim 40, Nguyen teaches the server being remotely located with respect to the switch

([0025-0029], Fig. 1-8)

17.   As per claim 41, Nguyen teaches the storage device being remotely located with respect to the

switch ([0025-0029], Fig. 1-8).

18.   As per claim 42, Nguyen teaches a method for use by a device in a system for storing and

accessing data, the method comprising:

receiving a packet from an initiator destined for a virtual target and formatted in accordance with

a first protocol ([0027], initiator is the DP processor(s), protocols includes SCSI / Fiber channels);

determining if said packet is a data packet or a control packet ([0027], if a desire rate is needed a

control packet is determined by the DP side and then forwarded to a central location, otherwise a regular

packet will be sent to the TDs);

forwarding said packet to a central processing unit if said packet is a control packet ([0027],

where the CP1 desires a certain speed/rate, and thus requesting for such allocation of rates at the

NSM/ACSC controller); and

sending the packet to a physical target formatted in accordance with a second protocol at wire

speed if said packet is a data packet ([0027], where the switch CP1 does not perform store and forward,

the data is directly passed to and from the TD1-TD5).

Claim Rejections - 35 USC § 103

19.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such
> that the subject matter as a whole would have been obvious at the time the invention was made to a person having
> ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in
> which the invention was made.

20.   Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blumenu in view

of Madonna et al. (hereinafter Madonna), US 5,596,569.

21.   As per claims 2 and 3, Blumenu disclose the invention substantially as rejected in claim 1 above,

but does not explicitly teach how to add/insert and/or remove a plurality of linecards.

However, Madonna teaches adding and/or removing a plurality of linecards (Madonna, Col. 7,

lines 20-24).

It would have been obvious to person of ordinary skill in the art at the time of the invention to

incorporate teaching of Madonna with Blumenu because the combination would improve the fault

tolerance of Blumenu's system by isolation of the linecards within the switch, leading to resiliency of

DSP and packet engine functions (Madonna, Col. 4, lines 15-25).

22.   Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blumenu in view

of Parthasarathy et al. (hereinafter Parthasarathy), US 6,831,916.

23.   As per claim 6, Blumenau discloses the invention substantially as rejected in claim 4 above, but

does not teach the infiniband protocol.

However, Parthasarathy teaches infiniband protocol (Col. 10, line 1).

It would have been obvious to person of ordinary skill in the art at the time of the invention to

incorporate teaching of Parthasarathy with Blumenu because the combination would improve the

efficiency of Blumenu's system by minimizing pipelining and data processing with minimal latency.

24.   Claims 7, 9-14, 16-17, 24-29, 32, 34, 43 and 44 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Blumenau, as applied to claims 1, 15, and 35 above, in view of Blumenau et al.

(hereinafter Blumenau 120') US 6,260,120.

25.   As per claims 7, 9 and 27, Blumenau discloses the invention substantially as rejected in claim 1

above, but does not teach receiving a packet at a first port of a first linecard destined for a virtual target

and formatted in accordance with a first protocol, determining if the packet is a data or control packet, and

if the packet is a data packet, sending the packet formatted in accordance with a second protocol to a

physical target, all without buffering the packet.

However, Blumenau '120 teaches it in the abstract, column 12, lines 9-15, column 13, lines 1-10. (Note, when the storage is denied the packet/data is a control packet to perform a function, data packet includes, but not limited to video data).

Thus, it would have been obvious to one skill in the art to combine Blumenau's inventions in order to minimize the number of servers by reducing the number of objects to be managed.

26.   As per claim 10, Blumenau – Blumenau '120 disclose the invention substantially as rejected in claim 1 above including receiving a packet at a first port of a first linecard destined for a virtual target and formatted in accordance with a first protocol, determining if the packet is a data or control packet, and if the packet is a data packet, sending the packet formatted in accordance with a second protocol to a physical target, all at wire speed (Blumenau '120, figures 1-4, 7, 21-30 and column 24, lines 56-67, columns 25 and 26).

27.   As per claim 11, Blumenau – Blumenau '120 disclose the invention substantially as rejected in claim 1 above including performing the storage service at request of a second device without any additional involvement of the second device (Blumenau '120, abstract).

28.   As per claim 12, Blumenau – Blumenau '120 disclose the invention substantially as rejected in claim 11 above including the second device being a server (Blumenau '120, abstract).

29.   As per claim 13, Blumenau – Blumenau '120 disclose the invention substantially as rejected in claim 11 above including the second device being a management station (Blumenau '120, abstract).

30.   As per claim 14, Blumenau – Blumenau '120 disclose the invention substantially as rejected in claim 11 above including the storage service is any one of local mirroring (Blumenau '120, Col. 20, lines 15-16), mirroring over slow link, snapshot, replication, third-party copy (Blumenau, Col. 4, lines 37-54), periodic backup, and restore.

31.   As per claim 16, Blumenau disclose the invention substantially as rejected in claim 15 above, but

does not teach each processing unit includes a packet aggregation aid classification unit and a packet-

processing unit, and associated with a memory.

However, Blumenau ('120) teaches the above in figures 1-4, 7, 21-30, which memories are

functionally equivalent to CAM and SRAM.

Thus, it would have been obvious to one skill in the ad to combine Blumenau's inventions in

order to minimize the number of servers by reducing the number of objects to be managed.

32.   As per claims 17, constructing formerly integral structure in various element and/or integrating

different parts in one, involves only routine skill in the art. Nrewin v. Erlichman, 168 USPQ 177, 179

and In re Hotte, 177 USPQ 326, 328 (CCPA 1973).

33.   As per claim 43, Blumenau does not teach:

receiving a packet from an initiator destined for a virtual target and formatted in accordance with

a first protocol;

determining if the packet is a data or control packet;

if a data packet, sending the packet to a physical target formatted in accordance with a second

protocol; and

wherein all of the above steps are performed without buffering.

However, Blumenau '120 teaches:

receiving a packet from an initiator destined for a virtual target and formatted in accordance with

a first protocol (Blumenau '120, Col. 9, lines 35-45; Col. 12, lines 9-16, where the packets are in a

predetermined format operated in plurality of protocols);

determining if the packet is a data or control packet (Blumenau '120, Col. 37, lines 55-67, where

the write access is a writing of data packet to the disks, a challenge response protocol is initiated in

response to the data packet);

if a data packet, sending the packet to a physical target formatted in accordance with a second

protocol (Blumenau '120, Col. 37, lines 55-67; Col. 40, lines 44-65, where the challenge response

protocol is implemented on the frame in order to authenticate the user); and

wherein all of the above steps are performed without buffering (Blumenau '120, Col. 16, lines 20-

25, lines 45-50, the cache 32 is the only memory subsystem within the cached storage subsystem to have

a cache of data, the purpose of this case is to speed up data access of popular data, and it's existence is

optional; Blumenau '120, Col. 25, lines 18-27; Col. 26, lines 1-25, the cache 32 is not used for direct

access of disk drives (28-31), the port adapter automatically creates virtual ports and linking the physical

ports to virtual ports in order for direct access to the disk volumes 28-31).

34.   As per claim 44, Blumenau – Blumenau '120 disclose the invention substantially as rejected in

claim 43 above, including the steps performed at wire speed (Blumenau, Fig. 1-5, Col. 5, lines 20-30).

35.   As per claim 24, the claim is rejected for the same reasons as rejection to claim 1 above, however,

Blumenau does not explicitly teach:

a plurality of initiators and targets;

wherein a first set of initiators and targets operate in accordance with a first protocol and a second

set of initiators and targets operate in accordance with a second protocol, and

wherein a third set of initiators and targets are local with respect to the switch and a fourth set of

initiators and targets are remote with respect to the switch.

However, Blumenau '120 teaches:

a plurality of initiators and targets (Fig 1, item 22-25, item 28-31, the two groups are be targets or initiators depending on read/write requests);

wherein a first set of initiators and targets operate in accordance with a first protocol and a second set of initiators and targets operate in accordance with a second protocol (Col. 9, lines 35-42), and

wherein a third set of initiators and targets are local with respect to the switch and a fourth set of initiators and targets are remote with respect to the switch (Fig 1, item 22-25, item 28-31, the two groups are be targets or initiators depending on read/write requests. That is, the hosts can send a read/write request and they are remote from the switch. Alternately, the disk drives 38-31 are local to the switch and they can be targets or initiators depending on read/write requests).

Thus, it would have been obvious to one skill in the art to combine Blumenau's inventions in order to minimize the number of servers by reducing the number of objects to be managed.

36.   As per claim 25, Blumenau – Blumenau '120 disclose the invention substantially as rejected in claim 24 above, including the first set, the second set, the third set, and the fourth set are not mutually exclusive (Blumenau '120, figures 1-4, 21-23, 37-40).

37.   As per claim 26, Blumenau – Blumenau '120 disclose the invention substantially as rejected in claim 24 above, including plurality of switches, each switch including a plurality of linecards, each linecard including a plurality of pods and a plurality of processing units, wherein each processing unit is associated with at least one port, wherein some of the switches are remotely located with respect to other switches (Blumenau '120, figures 1-4, 21-23, 37-40).

38.   As per claim 28, Blumenau – Blumenau '120 disclose the invention substantially as rejected in claim 24 above, including virtualization and translation, at wire speed (Blumenau '120, figures 1-4, 7, 21-30 and column 24, lines 56-67, columns 25 and 26).

39.   As per claim 29, Blumenau – Blumenau '120 disclose the invention substantially as rejected in

claim 24 above, including the packets formatted in accordance with any respective one of a plurality of

protocols (Blumenau, Col. 9, lines 35-43).

40.   As per claim 32, Blumenau – Blumenau '120 disclose the invention substantially as rejected in

claim 24 above, including plurality of switches, each including a plurality of linecards, each including a

plurality of ports and a plurality of processing units, wherein each processing unit is associated with at

least one port, and wherein additional/removed switches can be added to the plurality of switches

(Blumenau '120, figures 2, 38, 40, Col. 10, lines 5-13).

41.   As per claim 34, Blumenau – Blumenau '120 disclose the invention substantially as

rejected in claim 24 above, including plurality of switches, each switch including a plurality of linecards,

each linecard including a plurality of ports and a plurality of processing units, wherein each processing

unit is associated with at least one port, wherein only one management station is required to mange the

plurality of switches (Blumenau '120, figures 16 - where the system administrator grants access based on

his/her criteria).

42.   Claims 30, 31, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blumenau –

Blumenau '120, as applied in claim 24 above, in view of Madonna.

43.   As per claims 30, 31, 33, Blumenau – Blumenau '120 disclose the invention substantially as

rejected in claim 24 above, but does not teach how to add/insert and/or remove a plurality of linecards.

         However, Madonna teaches how to add and/or remove a plurality of linecards (Col. 7, lines 20-

24).

         Thus, it would have been obvious to one skill in the art to incorporate Madonna's architecture of

linecards with Blumenau – Blumenau '120's systems because the combination would improve the fault

tolerance of Blumenau – Blumenau '120's system by isolation of the linecards within the switch, leading

to resiliency of DSP and packet engine functions (Madonna, Col. 4, lines 15-25).

44.   Claims 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blumenau, as

applied to claims 15 and 21 above, in view of Nguyen.

45.   As per claim 19, Blumenau disclose the invention substantially as rejected in claim 15 above,

does not teach a traffic manager in communication with each processing unit.

However, Nguyen teaches the traffic manager in communication with each processing unit

(Nguyen paragraph (0030), figures 1-8).

Thus, it would have been obvious to one skill in the art to incorporate Nguyen with Blumenau

because the combination would improve the capabilities of Blumenau by allowing for controlling storage

device allocation and configuration and achieve the required data rate.   ,

46.   As per claim 22, Blumenau – Nguyen disclose the invention substantially as rejected in claim 21

above, including data packet virtualization (Nguyen, [0025-0028], [0037]).

47.   Claims 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blumenau – Nguyen, as

applied to claim 22 above, in view of Blumenau '120.

48.   As per claim 23, Blumenau – Nguyen disclose the invention substantially as rejected in claim 21

above, but does not explicitly say classifying packet as data packet or control packets.

Blumenau '120 teaches classifying packet as data packet or control packets (figures 1-4, 7, 21-30

and Col. 24, lines 56-67, columns 25 and 26, abstract, column 12, lines 9-15, Col. 13, lines 1-10. (Note,

when the storage is denied the packet/data is a control packet to perform a function, data packet includes,

but not limited to video data)).

Thus, it would have been obvious to one skill in the art to incorporate Blumenau '120 with

inventions with Blumenau – Nguyen because the combination would improve the efficiency of Blumenau
- Nguyen by minimizing the number of servers by reducing the number of objects to be managed.

49.   Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen, as applied in
claim 35 above, in view of Blumenau.

50.   As per claim 36, Nguyen discloses the invention substantially as rejected in claim 35 above, but
does not teach the plurality of linecards, each linecard including a plurality of ports and a plurality of
processing units, wherein each processing unit is associated with at least one port.

        However, Blumenau teaches plurality of linecards, each linecard including a
plurality of ports and a plurality of processing units, wherein each processing unit is associated with at
least one port (Blumenau, Col. 5, lines 13-31, and figures 1-3).

        Thus, it would have been obvious to one skill in the art to incorporate Blumenau with Nguyen's
system because the combination would improve the capabilities of Nguyen's system by minimize the
number of servers by reducing the number of objects to be managed.

51.   Claims 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen, as
applied in claim 35 above, in view of Blumenau '120.

52.   As per claim 37, Nguyen discloses the invention substantially as rejected in claim 35 above, but
does not teach a plurality of switches.

        However, Blumenau '120 teaches a plurality of switches (Blumenau '120, Col. 10, lines 5-8).

        Thus, it would have been obvious to one skill in the art to incorporate Blumenau '120 with
Nguyen's system because the combination would improve the capabilities of Nguyen's system by
minimize the number of servers by reducing the number of objects to be managed.

53.   As per claim 38, Nguyen - Blumenau '120 disclose the invention substantially as rejected in

claim 37 above, including only one management station is required to mange the plurality of switches

(Blumenau '120, Fig. 16, where the administrator grants access based on his/her criteria).

54.   As per claim 39, Nguyen - Blumenau '120 disclose the invention substantially as rejected in

claim 37 above, including the switches being remotely located with respect to other switches (Blumenau

'120, figures 2, 4, 21, 22, 37 and 38).

Response to Arguments

55.   In the remark, the applicant argued in substance:

a) As per claim 1, Blumenau does not teach "storage protocol processing units" that "perform

storage command processing".

b) As per claim 15, Blumenau does not teach "a fabric in communication with each linecard,

thereby allowing packets to pass from an ingress linecard to an egress linecard".

c) As per claim 21, Blumenau does not teach "means associated with each port for performing

wire speed processing of packets", "storage switch in accordance with an embodiment of the invention

will not buffer packets, unlike that done conventionally" (read into claim).

d) As per claim 20, Nguyen does not teach "a first CPU in communication with each processing

unit"

e) As per claim 20, Nguyen does not teach "each processing unit includes a classifier, a

virtualizer, and a translator".

f) As per claim 35, Nguyen does not teach "output for sending the data to a physical target

formatted in accordance with the second protocol at wire speed".

g) As per claim 43, Blumenau does not teach "wherein all the above steps are performed without buffering"

56.   In response to Applicant's arguments:

a) As per claim 1, Applicant does not disclose in the specification what is meant by "storage protocol", thus, in light of the specification and what is known in the art, SCSI and Fiber Channel are well known storage protocols used for storage access. Blumenau further teaches a plurality of storage protocol processing units (Col. 5, lines 12-27, where the storage adapters handles the *communications protocol of the storage devices* - emphasis added, each of the storage adapters has processors for handling the communications protocol of the storage devices, that is, Blumenau discloses *communications protocol of the storage devices* are FWD SCSI or Fibre Channel fiber-optic loops both are well known storage protocols), wherein each storage protocol processing unit is associated with at least one port and performs storage command processing for commands received at said at least one port (Col. 4, lines 37-54, Col. 5, lines 12-30, where storage adapters and port adapters are closely associated with each other, in order to effectively read and write information to and from cache and storage volumes), thereby distributing processing resources amongst linecard ports

b) As per claim 15, Blumenau teaches a fabric in communication with each linecard (Col. 6, lines 50-60; Fig 2, item 35, 36, and 40, where the adapter/linecards are connected to the port switch, which in turn provides fabric in communication with each linecard), thereby allowing packets to pass from an ingress linecard to an egress linecard.

c) As per claim 21, Blumenau teaches means associated with each port for performing wire speed processing of packets (Col. 5, lines 13-31, Fig 1-3, where the wire speed here is in accordance with the

line speed of the network, the processing speed is restricted by links between disks and storage adapters, i.e. FWD SCSI or Fiber Channel fiber-optic loops each have different speeds of access).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "storage switch in accordance with an embodiment of the invention will not buffer packets, unlike that done conventionally") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

d) As per claim 20, Nguyen teaches a first CPU in communication with each processing unit ([0027], where ACSC can be seen as the first CPU and processing units are combination of DP1-DP4 and CB1-CB4, the ACSC's CPU is in communications with each of the DP1 through DP4; alternately, each of combination of DP1-DP4 and CP1-CB4 can be seen as the CPU and CB5-CB9 can be considered as processing unit. Specifically, the translation from physical to virtual device can occur in connection blocks CB5-CB9 and in this case CB1-CB4 serve as a pass through function, where CB5 would serve the same function as CB-1 and CB-1 will act as a pass through device for the DP1 processor CPU);

e) As per claim 20, Nguyen teaches each processing unit includes a classifier, a virtualizer, and a translator ([0027], wherein the classifier, virtualizer and translator are achieved using data processors DP 1 through DP 9, though in one embodiment they are separate entities, however, in another embodiment, DP1-DP4 have functionalities of CB1-CB4, meaning they are integrated together into one unit and functionalities of CB1-CB4 are included within each of DP1-DP4, thus, Nguyen teaches processing units DP1-DP9 includes a classifier, a virtualizer, and a translator);

f) As per claim 35, Nguyen teaches the switch having an output for sending data for a virtual target formatted in accordance with the first protocol at wire speed ([0027], in one embodiment, CB1 will

act as a forwarding unit to forward the command to CB5, therefore, no buffering is done at the switch side, there are no store and forward at the switch).

g) As per claim 43, Blumenau '120 teaches wherein all of the above steps are performed without buffering (Blumenau '120, Col. 16, lines 20-25, lines 45-50, the cache 32 is the only memory subsystem within the cached storage subsystem to have a cache of data, the purpose of this case is to speed up data access of popular data, and it's existence is optional; Blumenau '120, Col. 25, lines 18-27; Col. 26, lines 1-25, the cache 32 is not used for direct access of disk drives (28-31), the port adapter automatically creates virtual ports and linking the physical.

57.   **THIS ACTION IS MADE FINAL.** Applicant is reined of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

58.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chad Zhong whose telephone number is (571)272-3946. The examiner can normally be reached on M-F 7:15 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JAROENCHONWANIT, BUNJOB can be reached on (571)272-3913. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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CZ

December 27, 2005

BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER